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EXAMINER
KAO, CHIH CHENG G

ART UNIT	PAPER NUMBER
2882	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/704,539	Applicant(s) KITAMURA ET AL.	
	Examiner Chih-Cheng Glen Kao	Art Unit 2882	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 April 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 4/18/03 has been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 6, 7, 11, 15, 16, 20, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (US Patent 6,157,072) in view of Takasaki et al. (US patent 4980736), Kobayashi et al. (US Patent 6476867), and Sugawa (US Patent 5869851).

3. With regards to claim 1, Nakayama et al. discloses a photoelectric conversion device (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, an energy level equal on the conduction or valence band side and discontinued on the other side, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C). Sugawa teaches the change of energy levels of approximately energy level equal on the conduction or valence band side and discontinued on the other side (Figs. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have energy levels as seen in Sugawa with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the energy levels to control the flow of current better as implied from Figures 5 and 6 of Sugawa. Note that the entire structure is known in the prior art and a recitation with respect to

the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

4. With regards to claim 4, Nakayama et al. discloses a photoelectric conversion device (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. and Sugawa teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to restriction of holes and electrons of Sugawa with the device of Nakayama et al., since one would be motivated to block the flow in one direction to have a multiplication effect in the other direction as implied from Sugawa (Fig. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

5. With regards to claim 6, Nakayama et al. discloses a photoelectric conversion device (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c)

a metal substrate (col. 20, lines 48-55),

accumulation units and output (col. 15, lines 63-65).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, an energy level equal on the conduction or valence band side and discontinued on the other side, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C). Sugawa teaches the change of energy levels of approximately energy level equal on the conduction or valence band side and discontinued on the other side (Figs. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have energy levels as seen in Sugawa with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the energy levels to control the flow of current better as implied from Figures 5 and 6 of Sugawa. Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

6. With regards to claim 7, Nakayama et al. discloses a photoelectric conversion device (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. and Sugawa teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to restriction of holes and electrons of Sugawa with the device of Nakayama et al., since one would be motivated to block the flow in one direction to have a multiplication effect in the other direction as implied from Sugawa (Fig. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the

prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

7. With regards to claim 11, Nakayama et al. further discloses a metal substrate (col. 20, lines 48-55).

8. With regards to claim 15, Nakayama et al. further discloses the layer structure consisting of the carrier generation/multiplication, electron injection inhibiting, and hole injection inhibiting layer (Fig. 3).

9. With regards to claim 16, Nakayama et al. discloses a solid state image sensing device comprising photoelectric conversion devices (Title and Fig. 1b) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c),

accumulation units and output (col. 15, lines 63-65).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, an energy level equal on the conduction or valence band side and

discontinued on the other side, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C). Sugawa teaches the change of energy levels of approximately energy level equal on the conduction or valence band side and discontinued on the other side (Figs. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have energy levels as seen in Sugawa with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the energy levels to control the flow of current better as implied from Figures 5 and 6 of Sugawa. Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in

the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

10. With regards to claim 20, Nakayama et al. further discloses the layer structure consisting of the carrier generation/multiplication, electron injection inhibiting, and hole injection inhibiting layer (Fig. 3).

11. With regards to claim 25, Nakayama et al. discloses a solid state image sensing device comprising photoelectric conversion devices (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c),

accumulation units and output (col. 15, lines 63-65).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. and Sugawa teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to restriction of holes and electrons of Sugawa with the device of Nakayama et al., since one would be motivated to block the flow in one direction to have a multiplication effect in the other direction as implied from Sugawa (Fig. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

12. With regards to claim 26, Nakayama et al. discloses a solid state image sensing device comprising photoelectric conversion devices (Title) having a layered structure comprising or consisting:

an amorphous silicon layer to absorb light and generate carriers (Fig. 3, #30b, 32b),

an amorphous silicon carbide of p-type conductivity layer (Fig. 3, #30a, 32a),

an amorphous silicon nitride (col. 20, lines 34-46) of n-type conductivity layer (Fig. 3, #30c, 32c),

accumulation units and output (col. 15, lines 63-65).

However, Nakayama et al. does not specifically disclose silicon as a multiplication layer and inhibiting layers, and prevention of holes or electrons flowing and electron or hole injection thereto.

Takasaki et al. teaches silicon as a multiplication layer (col. 4, lines 64-65) and inhibiting layers (col. 1, lines 35-40, and col. 4, lines 64-69). Kobayashi et al. and Sugawa teaches prevention of holes or electrons flowing and electron or hole injection thereto (Fig. 10A-10C).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the multiplication layer and inhibiting layers of Takasaki et al. with the device of Nakayama et al., since one would be motivated to have low dark current as shown by Takasaki et al. (col. 3, lines 17-20, and col. 4, lines 58-69).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to restriction of holes and electrons of Sugawa with the device of Nakayama et al., since one would be motivated to block the flow in one direction to have a multiplication effect in the other direction as implied from Sugawa (Fig. 5 and 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have restricted flow of holes and electrons as seen in Kobayashi et al. with the device of Nakayama et al., since where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to manipulate the flow to create different modes of the circuit as implied from Kobayashi et al. (col. 8, lines 9-15). Note that the entire structure is known in the prior art and a recitation with respect to the manner in which a claimed apparatus is intended to employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

13. Claims 2, 5, 17, 18, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa as applied to claims 1, 4, 6, 7, 25, and 26, and further in view of Deane et al. (US patent 6064091).

14. With regards to claims 2 17, and 24, Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa suggest a device as recited above.

However, Nakayama et al. does not seem to specifically disclose a ratio C/Si of 1.5 or lower.

Deane et al. teaches a ratio C/Si of 1.5 or lower.

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the ratios of Deane et al. with the device of Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa, since where the general conditions of a claim

are disclose in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to have the band gap to allow excess carriers to move easily as shown by Deane et al. (col. 2, lines 35-41).

15. With regards to claims 5, 18, and 23, Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa suggest a device as recited above.

However, Nakayama et al. does not seem to specifically disclose a ratio N/Si of 0.8 or lower.

Deane et al. teaches a ratio N/Si of 0.8 or lower. (col. 5, lines 27-31).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the ratios of Deane et al. with the device of Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa, since where the general conditions of a claim are disclose in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. One would be motivated to have the band gap to allow excess carriers to move easily as shown by Deane et al. (col. 2, lines 35-41).

16. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa as applied to claim 1 and 4 above, and further in view of Anagnostopoulos (US Patent 5563404), Ota (US Patent 4496981), and Waki et al. (JP 01-311511).

Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa suggest a device as recited above.

However, Nakayama et al. does not disclose a substrate comprising polycrystalline, microcrystalline, or monocrystalline silicon.

Anagnostopoulos teaches monocrystalline silicon (Claim 2). Ota teaches polycrystalline silicon (col. 2, lines 53-61). Waki et al. teaches polycrystalline and microcrystalline silicon (Abstract, Constitution).

It would have been obvious to one having ordinary skill in the at the time the invention was made, to have those substrates with the materials of Anagnostopoulos, Ota, and Waki et al. with the device of Nakayama et al. in view of Takasaki et al., Kobayashi et al. and Sugawa, which is explained as follows. Since these materials are considered conventional functionally equivalent as relatively inflexible materials, it would have been within routine skill for one having ordinary skill in the art to place the device on any material that was inflexible. It would have been within routine skill to substitute one type of material for another as shown by Nakayama et al. (col. 20, lines 48-56). Also it is within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. One would be motivated to use those materials because they don't bend and provide support as implied from Anagnostopoulos, Ota, and Waki et al.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa as applied to claim 4, and further in view of Fukuda et al. (US patent 5635327).

Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa suggest a device as recited above.

However, Nakayama et al. does not disclose boron in the carrier generation layer.

Fukuda et al. teaches boron in the carrier generation layer (col. 4, lines 48-57).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the boron of Fukuda et al. with the device of Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa, since one would be motivated to control dark resistance as shown by Fukuda et al. (col. 4, lines 48-57) which is related to the dark current.

18. Claims 13, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kozuka et al. (JP 09-102627), and Kobayashi et al.

For purposes of being concise, Nakayama et al. in view of Takasaki et al. suggests a device as recited above.

However, Nakayama et al. does not disclose an electric field reducing layer between a carrier generation/multiplication layer and hole or electron injection inhibiting layer.

Kozuka et al. teaches an electric field reducing layer between a carrier generation/multiplication layer and charge injection inhibiting layer (Abstract). Kobayashi et al. teaches the charge injection inhibiting layers as hole or electron.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have electric field reducing layer of Kozuka et al. with the device of Nakayama et al. in view of Takasaki et al., since one would be motivated to reduce dark current as implied from Kozuka et al. (Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have charge injection inhibiting layers as hole or electron of Kobayashi et al. with the device of Nakayama et al. in view of Takasaki et al. and Kozuka et al., which is explained with motivation as follows. Since these two elements were art-recognized equivalents at the time the invention was made as shown by Kabayashi et al. (col 2, lines 34-37), it would be obvious to put the electric field reducing layer between the carrier generation/multiplication layer and either hole or electron injection inhibiting layer in order to reduce dark current as implied from Kobayashi et al. (col. 2, lines 1-7 and 20-40).

19. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al.

For purposes of being concise, Nakayama et al. in view of Takasaki et al. suggest the device as recited above.

However, Nakayama et al. does not disclose the inhibiting layer on only a substrate.

Takasaki et al. further teaches the inhibiting layer (Fig. 1A, #15) on only a substrate (Fig. 1A, #16).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have inhibiting layer on only a substrate of Takasaki et al. with the device of Nakayama et al. in view of Takasaki et al., since one would be motivated place the inhibiting layer on something like a substrate for support as implied from Figure 1A of Takasaki et al.

20. Claims 27-30, 33, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa as applied to claims 1, 4, 6, 7, 16, 25, and 26 above, and further in view of Kodama et al. (US Patent 5122431).

Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa suggests a device as recited above.

However, Nakayama et al. does not specifically disclose the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity.

Kodama et al. teaches the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity (col. 1, lines 25-30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity of Kodama et al. with the suggested device of Nakayama et al. in view of Takasaki et al., Kobayashi et al., and Sugawa, since one would be motivated to incorporate it for carrier injection, which is used in forming an image as implied from Kodama et al. (col. 1, lines 13-34).

21. Claims 31, 32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kozuka et al., and Kobayashi et al. as applied to claims 13, 14, and 19 above, and further in view of Kodama et al.

Nakayama et al. in view of Takasaki et al., Kozuka et al., and Kobayashi et al. suggests a device as recited above.

However, Nakayama et al. does not specifically disclose the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity.

Kodama et al. teaches the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity (col. 1, lines 25-30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity of Kodama et al. with the suggested device of Nakayama et al. in view of Takasaki et al., Kozuka et al., and Kobayashi et al., since one would be motivated to incorporate it for carrier injection, which is used in forming an image as implied from Kodama et al. (col. 1, lines 13-34).

22. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al. as applied to claims 21 and 22 above, and further in view of Kodama et al.

Nakayama et al. in view of Takasaki et al. suggests a device as recited above.

However, Nakayama et al. does not specifically disclose the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity.

Kodama et al. teaches the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity (col. 1, lines 25-30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made, to have the amorphous silicon nitride of n-type conductivity as hydrogenated amorphous silicon nitride of n-type conductivity of Kodama et al. with the

suggested device of Nakayama et al. in view of Takasaki et al., since one would be motivated to incorporate it for carrier injection, which is used in forming an image as implied from Kodama et al. (col. 1, lines 13-34).

Response to Arguments

23. Applicant's arguments with respect to claims 27-38 have been considered but are moot in view of the new ground(s) of rejection.

24. Applicant's arguments filed 4/18/03 have been fully considered but they are not persuasive.

With regards to Nakayama et al., the combination is taught (col. 16, lines 47-60, and col. 20, lines 33-47).

With regards to Sugawa, Sugawa does teach claimed limitations regarding energy levels (Figs. 5 and 6). See col. 3, line 60, to col. 4, line 50 for further detail.

With regards to Deane, the reference does relate to photoelectric conversion devices (col. 1, lines 15-20) and includes a sandwich structure (Fig. 1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Cheng Glen Kao whose telephone number is (703) 605-5298. The examiner can normally be reached on M - F (9 am to 5 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Glick can be reached on (703) 308-4858. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

gk
June 23, 2003

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